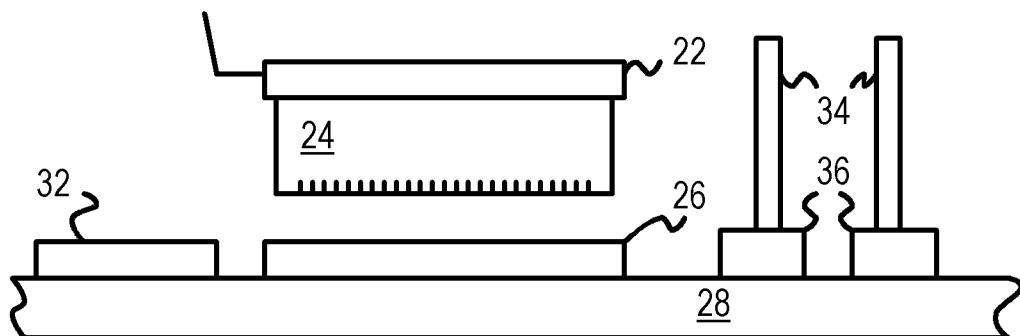


FIG. 1A



PRIOR ART

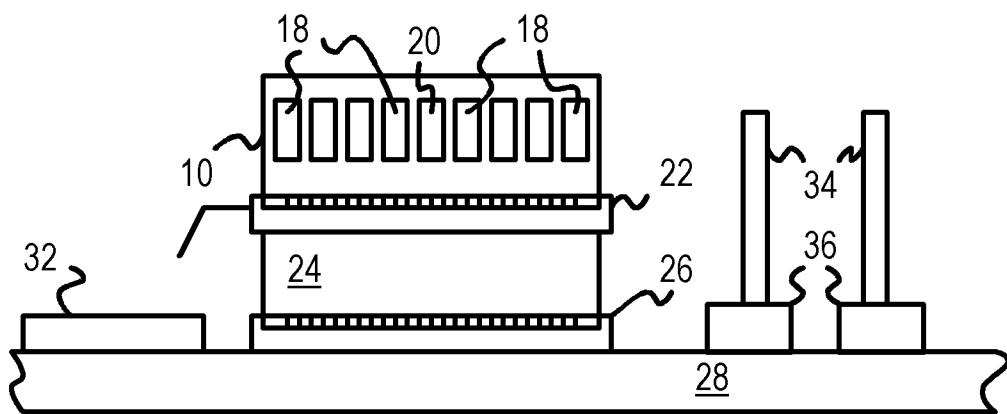
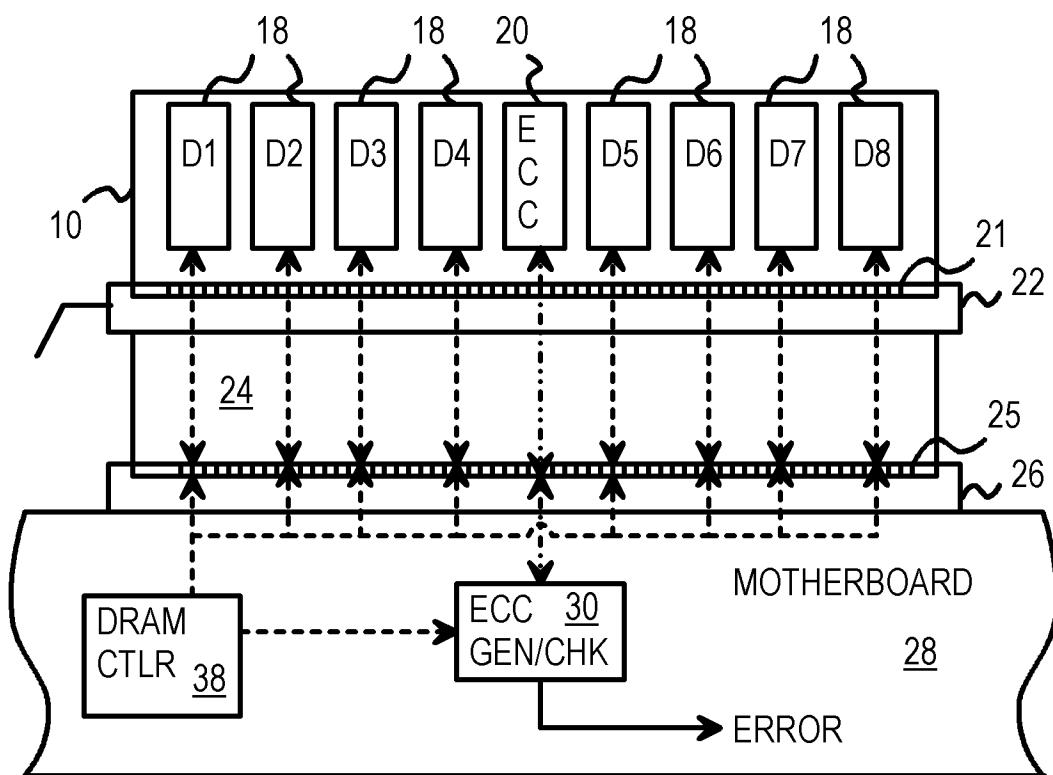
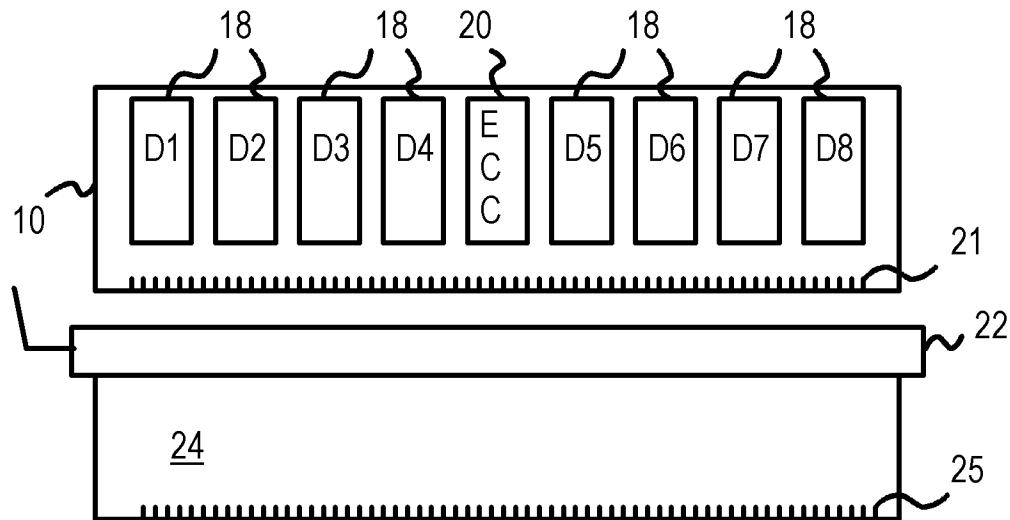


FIG. 1B

PRIOR ART

**FIG. 2A**

PRIOR ART



**FIG. 2B**

PRIOR ART

DATA DRAMs				ECC DRAM
D1	D2	D3	D4	ECC
1010	1010	1010	1010	0011
0101	0101	0101	0101	0001
1010	1010	1010	1010	0011
0101	0101	0101	0101	0001

**FIG. 3**  
PRIOR ART

DATA DRAMs				ECC DRAM
D1	D2	D3	D4	ECC
1010	1010	1010	0011	1010
0101	0101	0101	0001	0101
1010	1010	1010	0011	1010
0101	0101	0101	0001	0101

**FIG. 6**

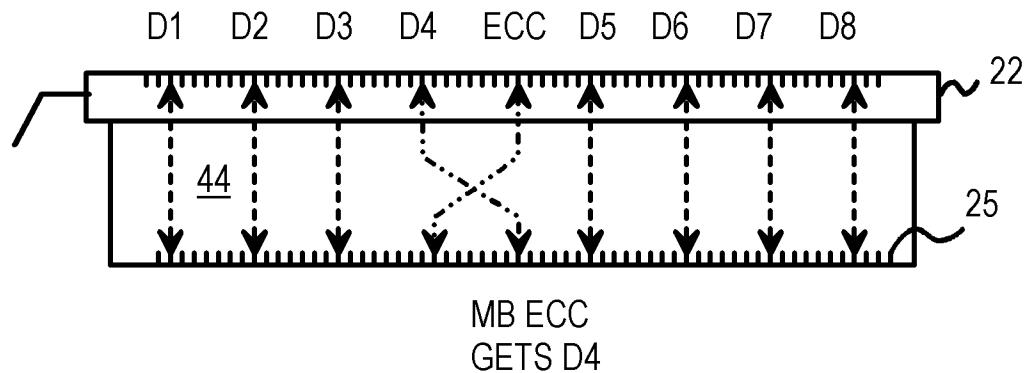


FIG. 4

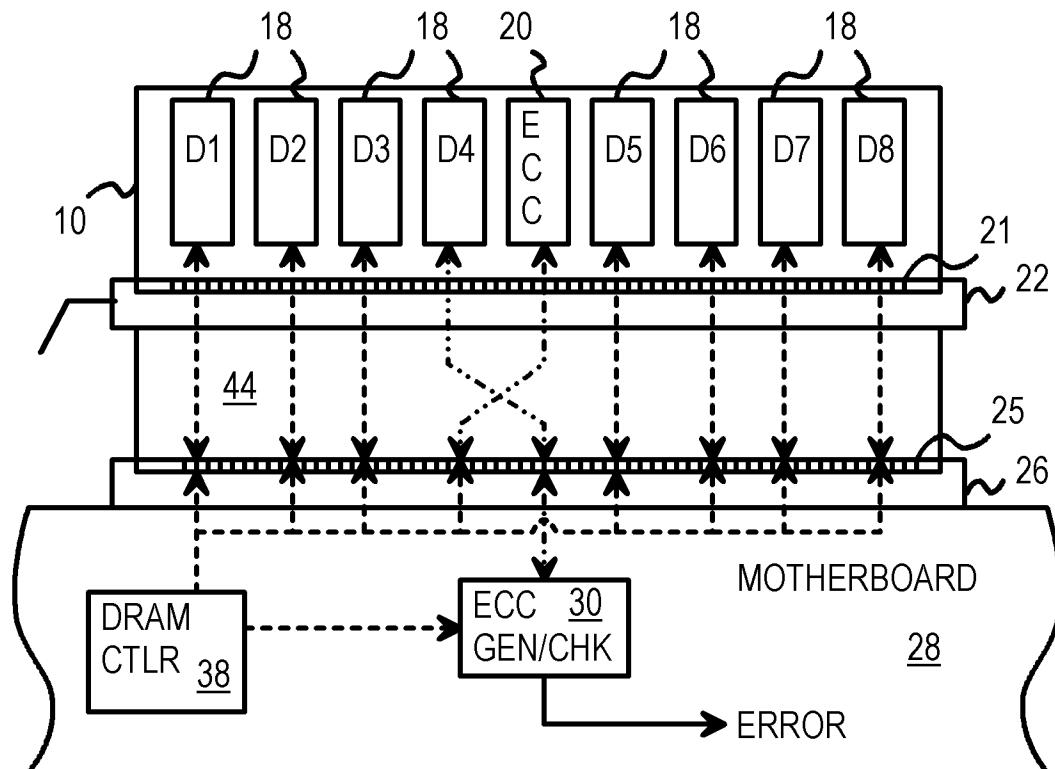


FIG. 5

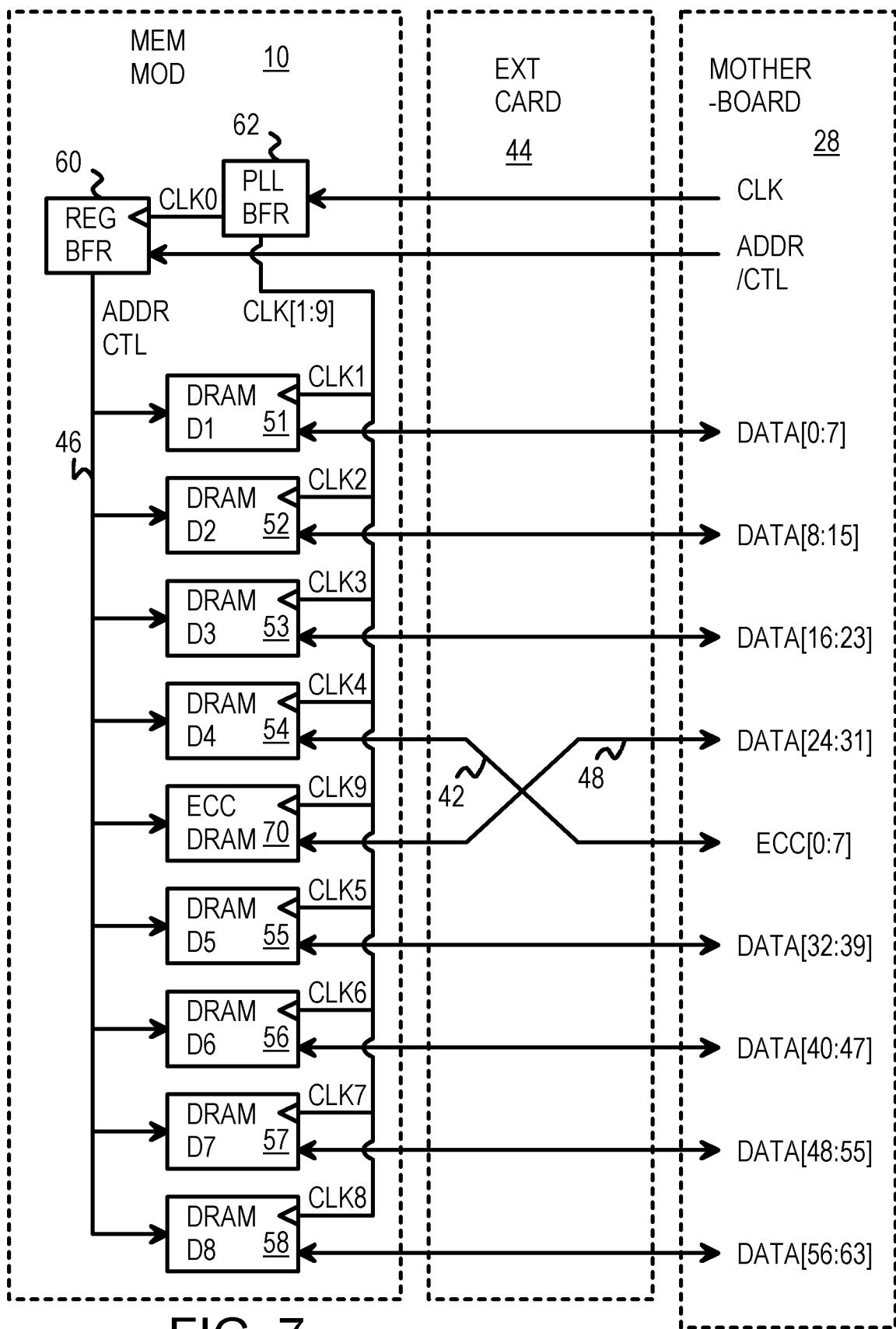


FIG. 7

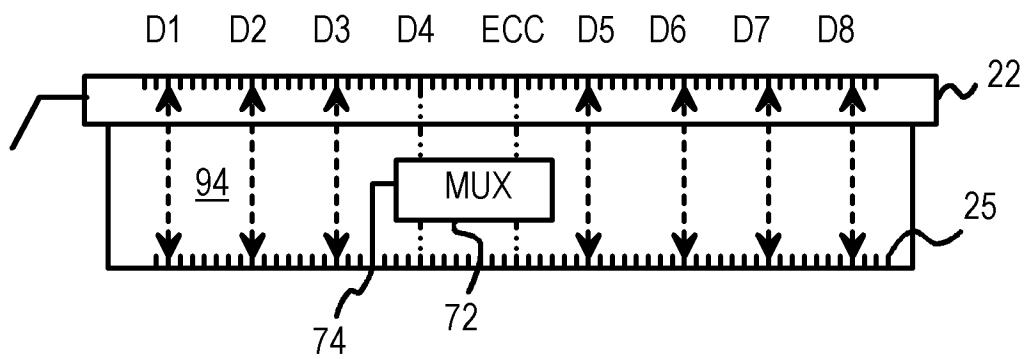


FIG. 8